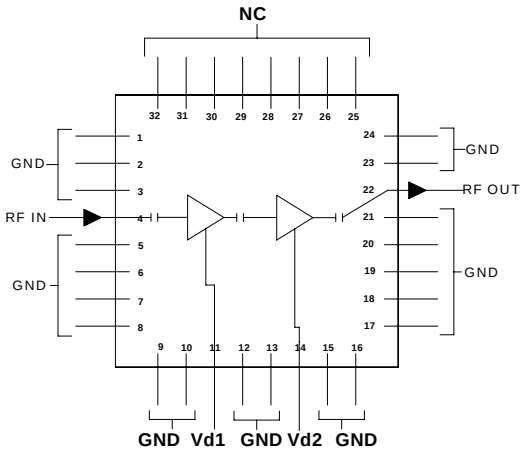
2.7 – 3.7 GHz Low Noise Amplifier

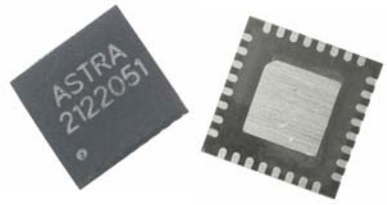
Features

- **Frequency Range : 2.7 – 3.7GHz**
- **Low Noise Figure < 1.6 dB**
- **23 dB High gain**
- **19 dBm Medium Power output**
- **High IP3**
- **Input Return Loss > 6 dB**
- **Output Return Loss > 10 dB**
- **Single supply operation**
- **No external matching required**
- **DC decoupled input and output**
- **0.15 µm InGaAs pHEMT Technology**
- **QFN Plastic package : 5mm x 5mm x 1mm**



Typical Applications

- **RADAR**
- **Military & space**
- **VSAT**



Description

The ASTRA 2122051P is S-band Low noise amplifier available in a low-cost QFN package for surface mount applications. The LNA uses 2 stages of amplification and operates in 2.7 – 3.7 GHz frequency range. The LNA features 23 dB of gain with a low noise figure of 1.6 dB and typical input and output return losses of 6 dB and 10 dB respectively. The LNA is unique in delivering a medium power output of 19 dBm. This feature enables it to be used in high gain applications with enhanced linearity requirements. The chip operates from a single positive supply voltage.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+6	volts
RF input power (RFin at Vd=4V)	18	dBm
Operating temperature	-50 to +85	^{o}C
Storage Temperature	-65 to +150	^{o}C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications [1] @ T_A = 25 °C, V_{d1} = 3V, V_{d2} = 4V Z_o =50 Ω

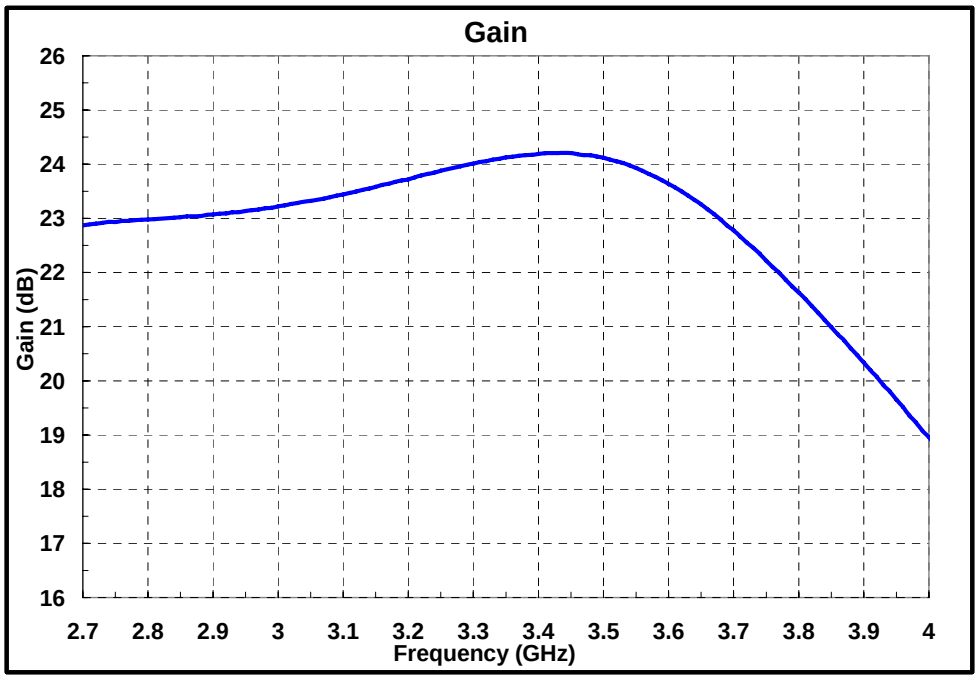
Parameter	Typ.			Units
Frequency Range	2.7 – 3.1	3.1 – 3.5	2.7 - 3.7	GHz
Gain	23	23.75	23.5	dB
Gain Flatness	± 0.25	± 0.4	± 0.6	dB
Noise Figure (max.)	1.4	1.6	1.6	dB
Input Return Loss (min.)	5	11	5	dB
Output Return Loss (min.)	15	12	9	dB
Output Power (P1 dB)	18	19	18	dBm
Saturated output power (Psat)	-	21	-	dBm
Output Third Order Intercept (IP3)	-	30	-	dBm
Supply Current	-	110	-	mA

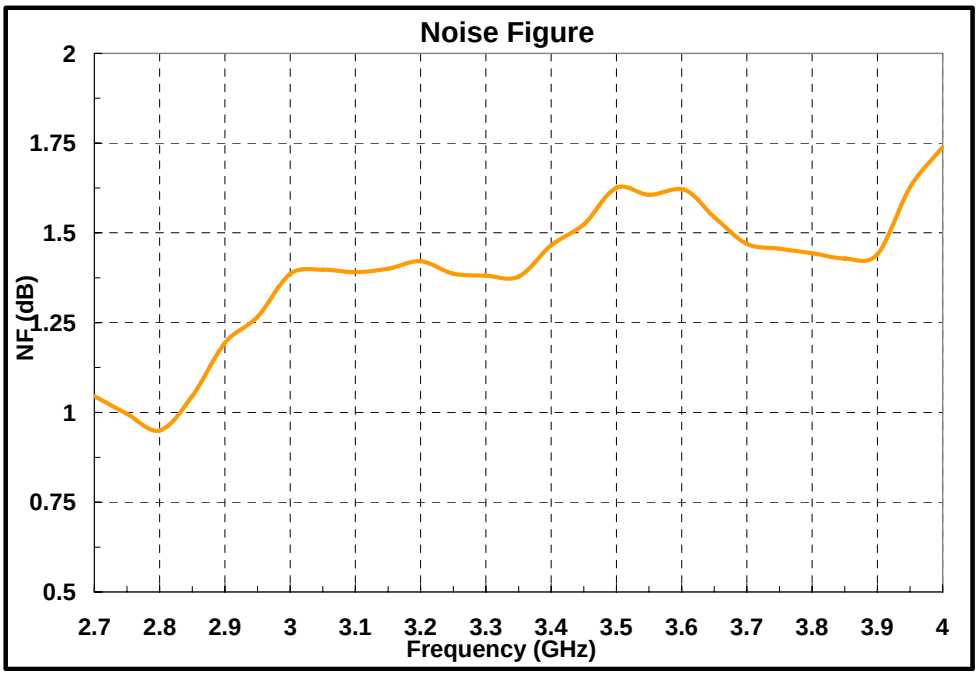
Note:

1. Electrical specifications are measured in a test fixture.

Test fixture data

Vd1 = 3V, Vd2 = 4V, Total Current = 110mA, T_A = 25 °C





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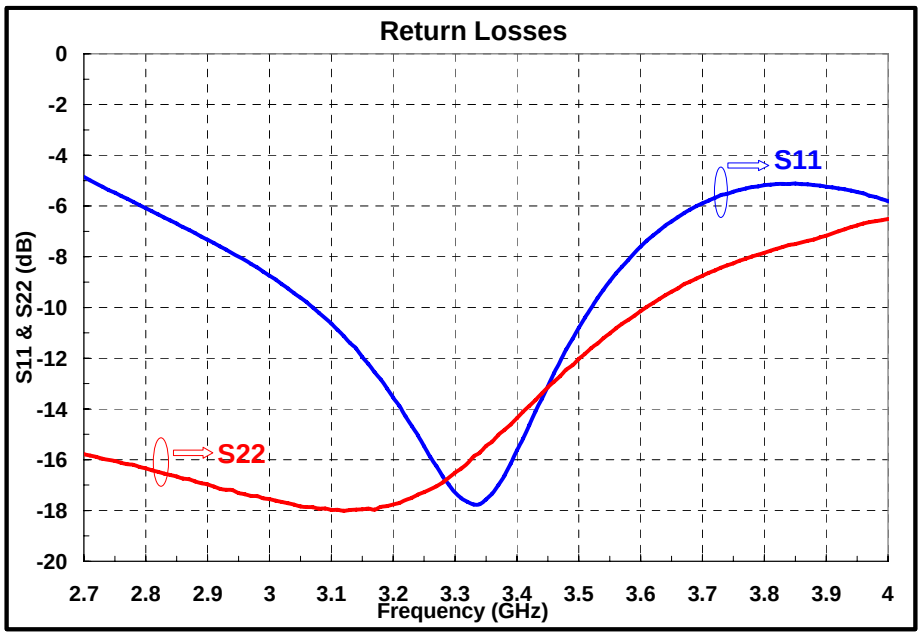

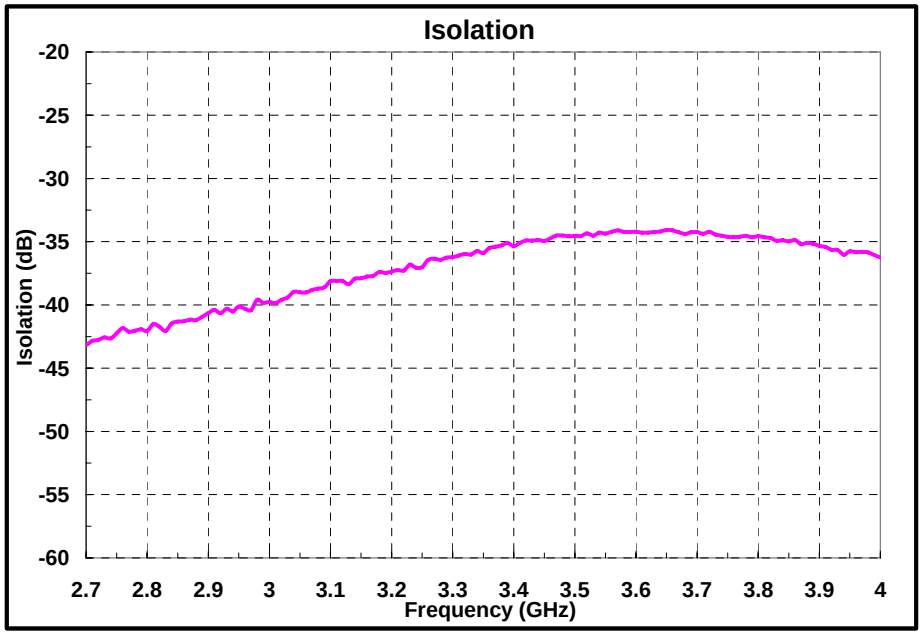

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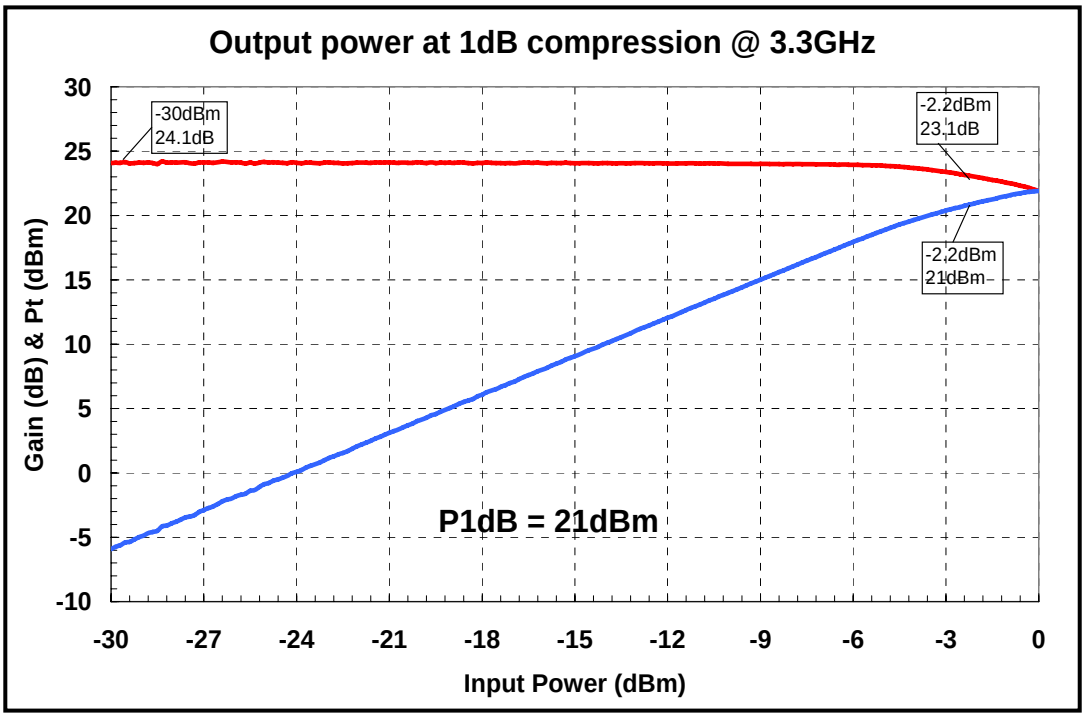
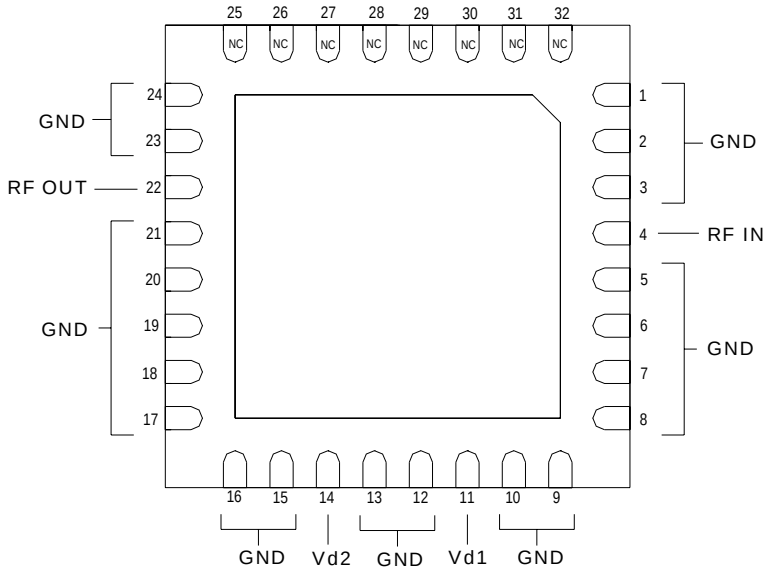


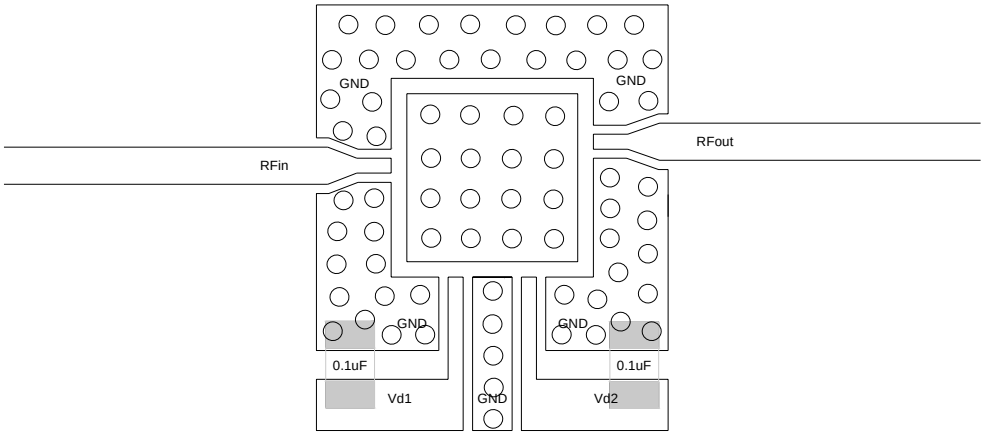
Pin Configuration



Pin Designations

Symbol	Pin No.	Description
GND	1,2,3,5,6,7,8,9,10,12,13,15,16,17,18,19,20,21,23,24	Grounded
RF IN	4	RF Input
RF OUT	22	RF Output
Vd1	11	1st Stage drain voltage
Vd2	14	2nd Stage drain voltage
NC	25,26,27,28,29,30,31,32	No Connection

Test Board Pattern



QFN mounted on test pattern

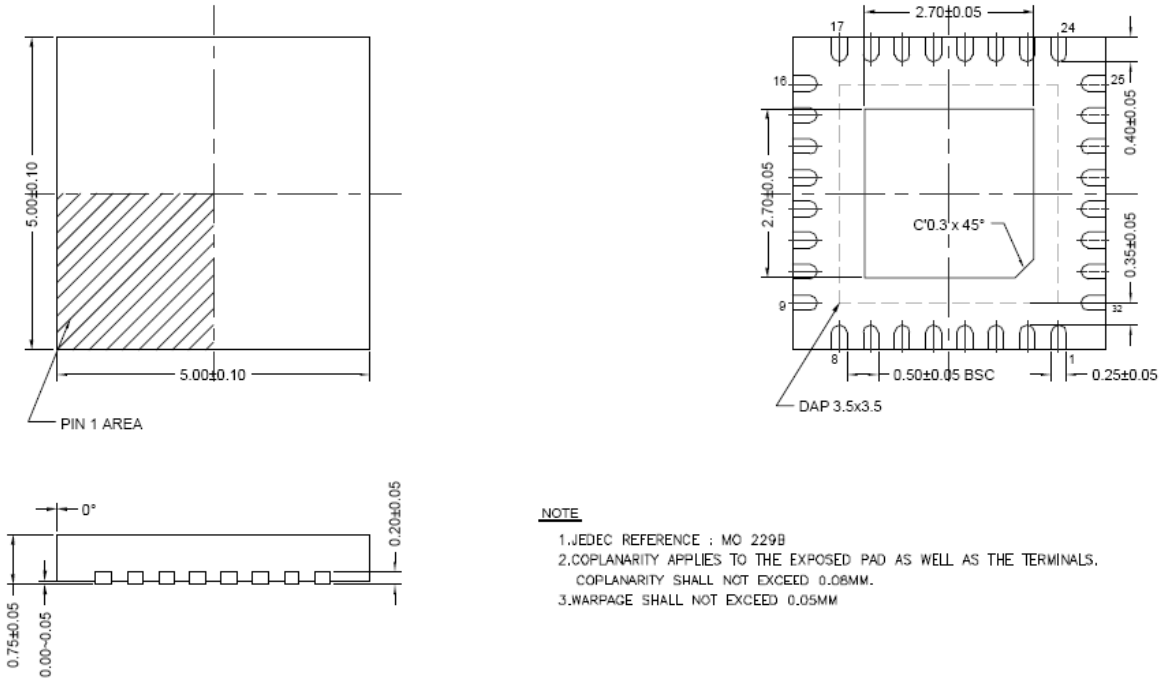
List of components

Capacitor value	Reference
0.1µF	0603

Note:

1. Input and output 50 ohm lines are on 10 mil RT duroid substrate
2. 0.1 µF capacitors may be additionally used as a second level of bypass for reliable operation

QFN package outline



NOTE
1.JEDEC REFERENCE : MO 229B
2.COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08MM.
3.WARPAGE SHALL NOT EXCEED 0.05MM

All units are in millimeters

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice